Wide Band-Gap Semiconductor Amplifiers for Plasma Heating and Control

Michael Paluszek (PFS), Dr. Christopher Galea (PFS), Dr. Minjie Chen (Princeton University), Dr. Peter Losee (Qorvo), Dr. Sreekant Narumanchi (NREL)

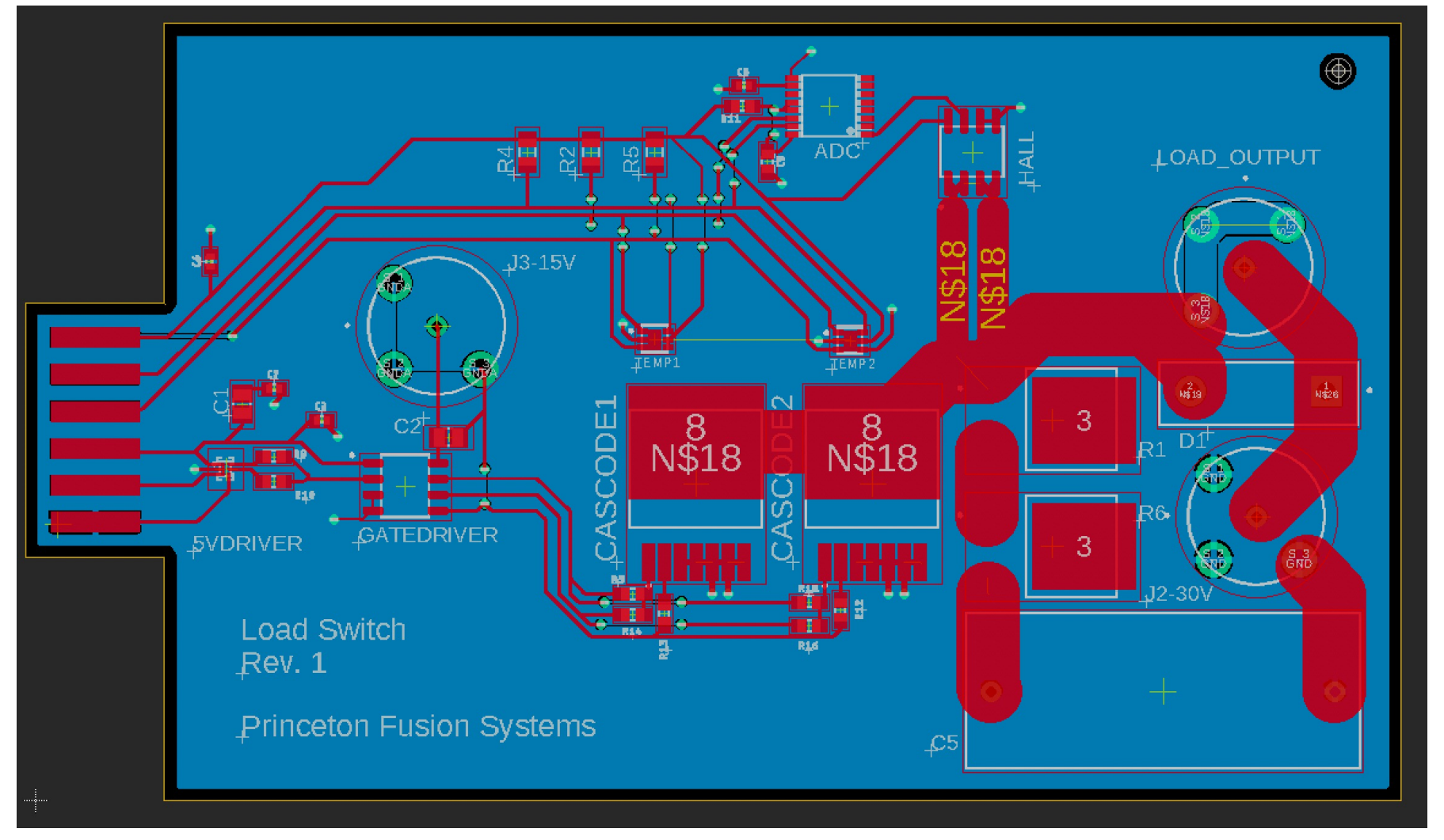
Motivation and Approach

The path towards fusion power net gain requires high wall-plug efficiencies. The growing R&D on wide bandgap (WBG) semiconductors shows promise for using these devices to enable high-efficiency power electronics. Utilizing WBG semiconductors, we are developing boards for three applications: short high power pulses (~5 μs), control pulses (~1 ms) and RF amplifiers (10's of MHz).

Wide Band Gap Devices

- Silicon carbide (SiC) and Gallium nitride (GaN)
- Faster switching (up to 10's of MHz)
- Less sensitive to temperature
- High voltages and currents
  - 2 kV SiC cascodes
- Higher reliability and efficiency

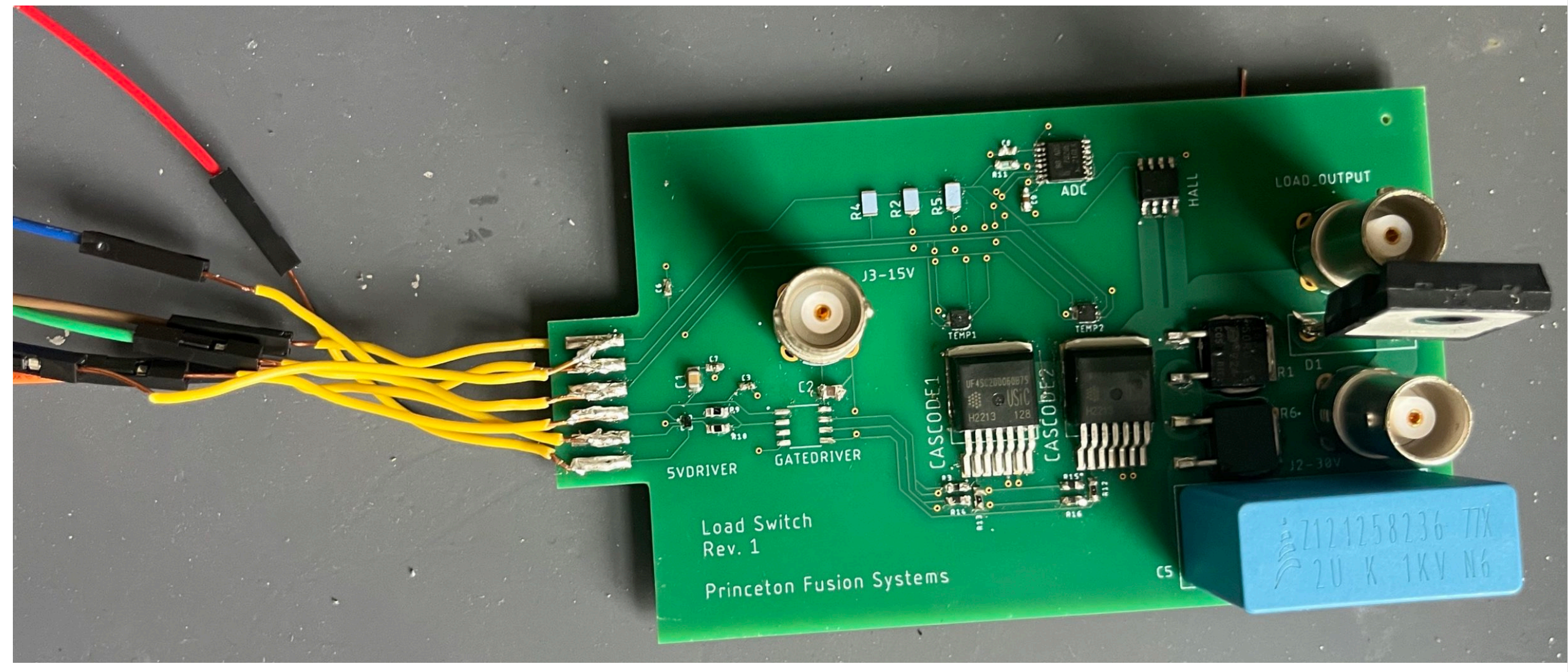
Load switch board layout



Advanced Board Design

- Plug and play for cooling and power
- Fault tolerant
- Fault detection and prediction
- Distributed signal generation

Load switch board prototype



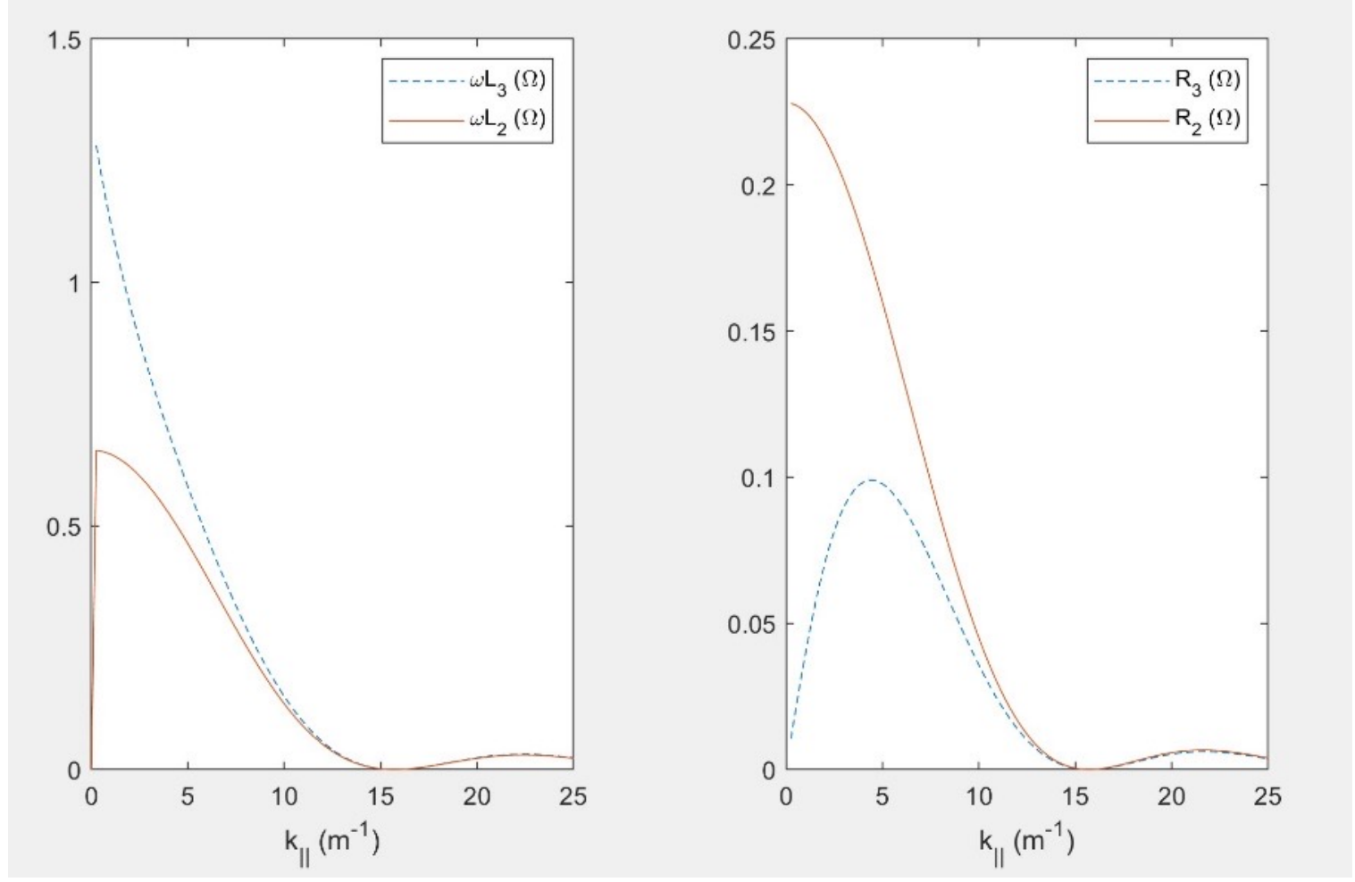
High Power Pulses

- Low-side load switch: prototype built
- H bridge
  - Multiple Qorvo cascodes

Plasma Circuit Model

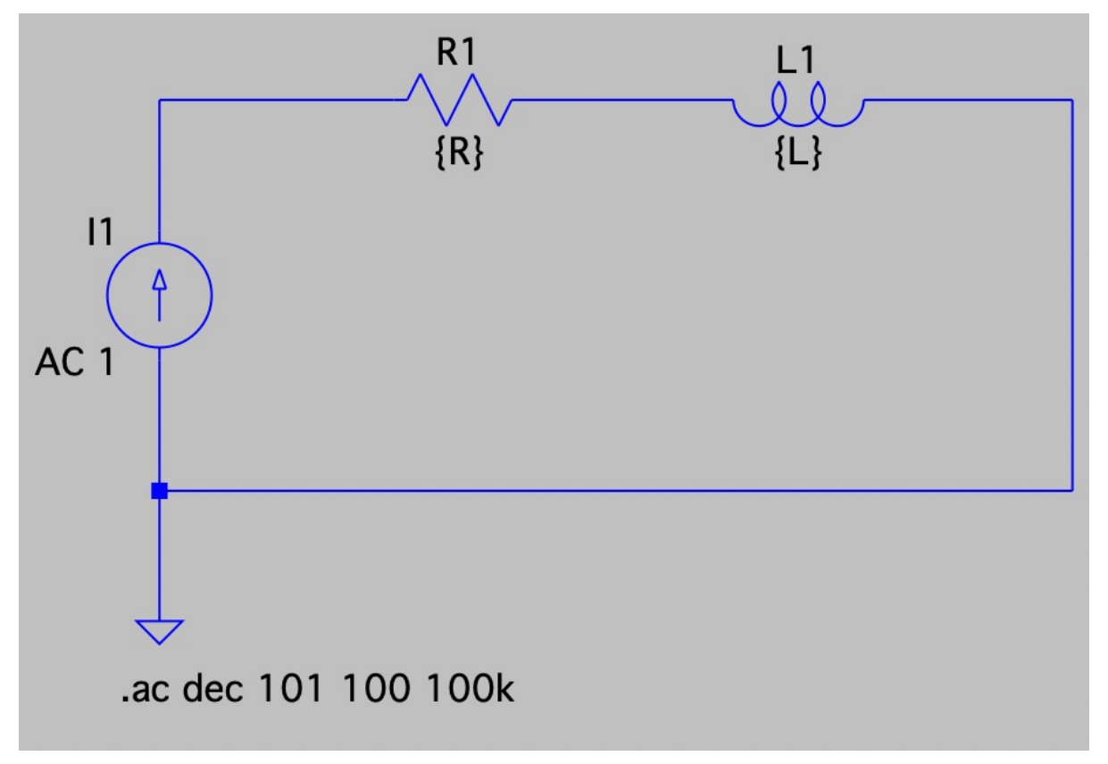
- Advances made in model which inputs parameters such as plasma density and temperature to make equivalent circuit for optimizing amplifier design

Plasma parameter inputs (e.g., number density)



PSS ICRH model based on Ref. [1]. Antenna reactance (left) and resistance (right).

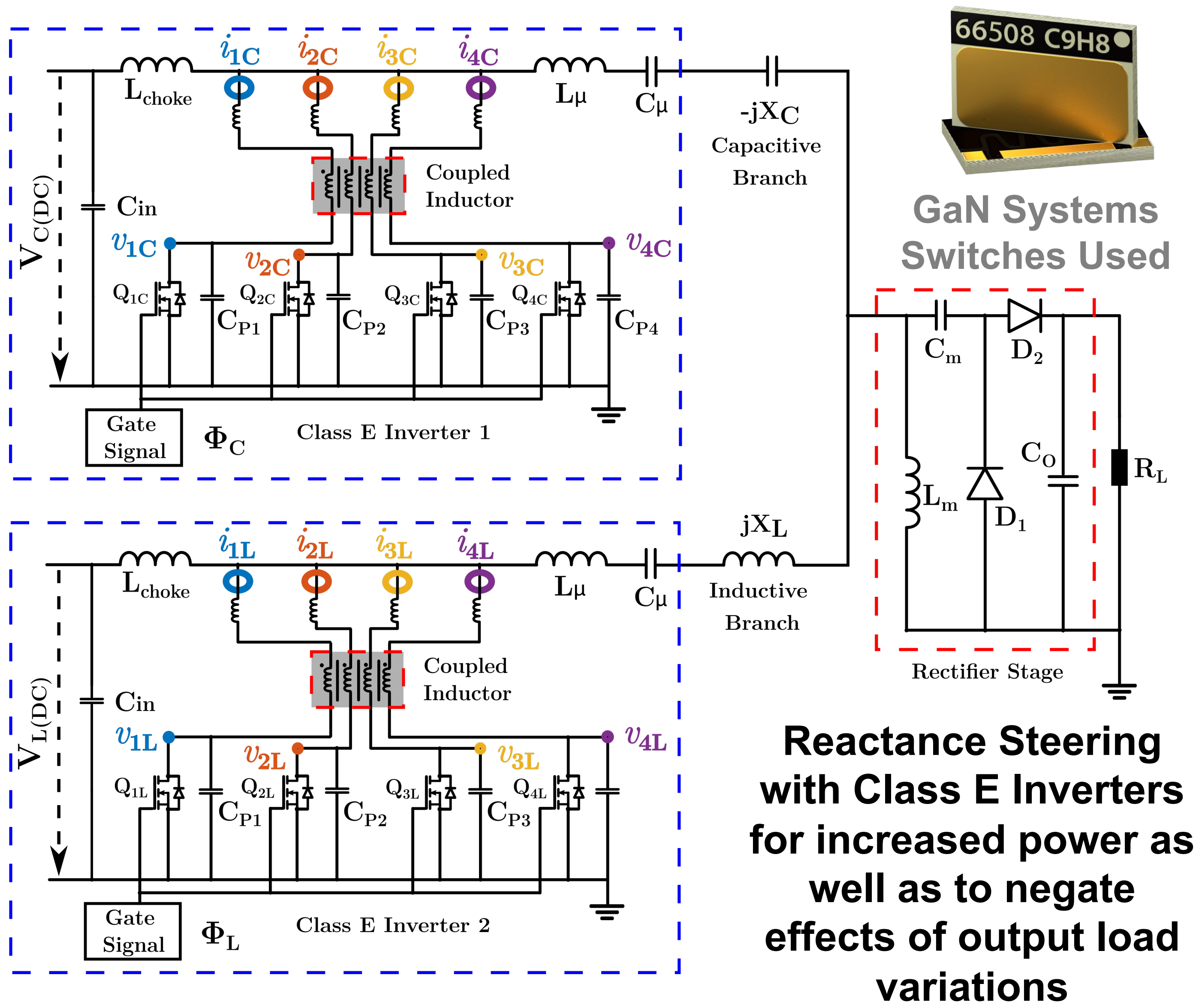
Impedance outputs: R, L



Simple LTSpice model to test running a batch of simulations given varying model impedance outputs

[1] Bhatnagar et al., "A 3-D analysis of the coupling characteristics of ion cyclotron resonance heating antennae," *Nuclear Fusion* 22, 280 (1982).

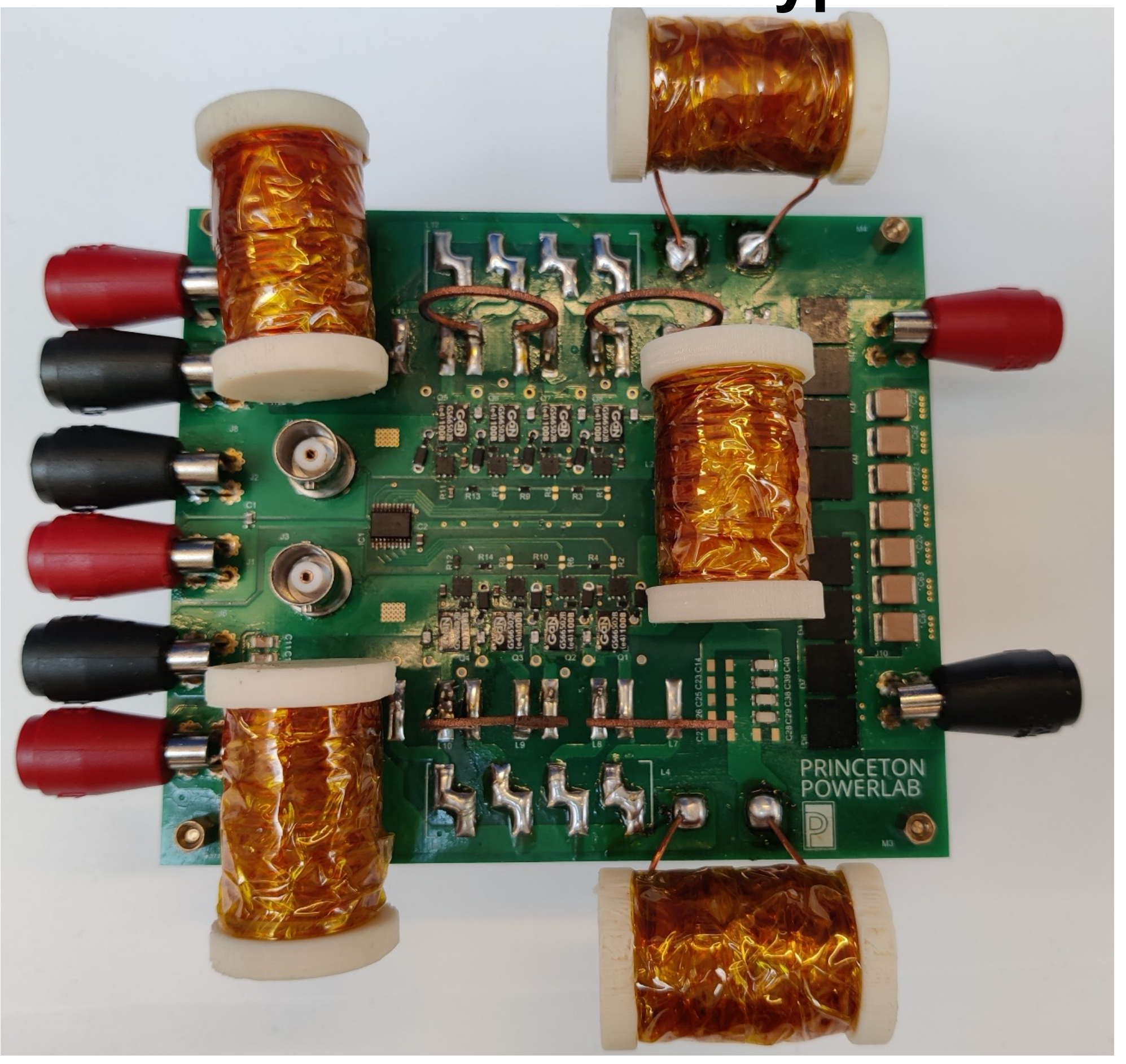
Radio-Frequency Heating



GaN Systems Switches Used

Reactance Steering with Class E Inverters for increased power as well as to negate effects of output load variations

Hardware Prototype



Operated at 10MHz, output power of 200W with ZVS in all switches

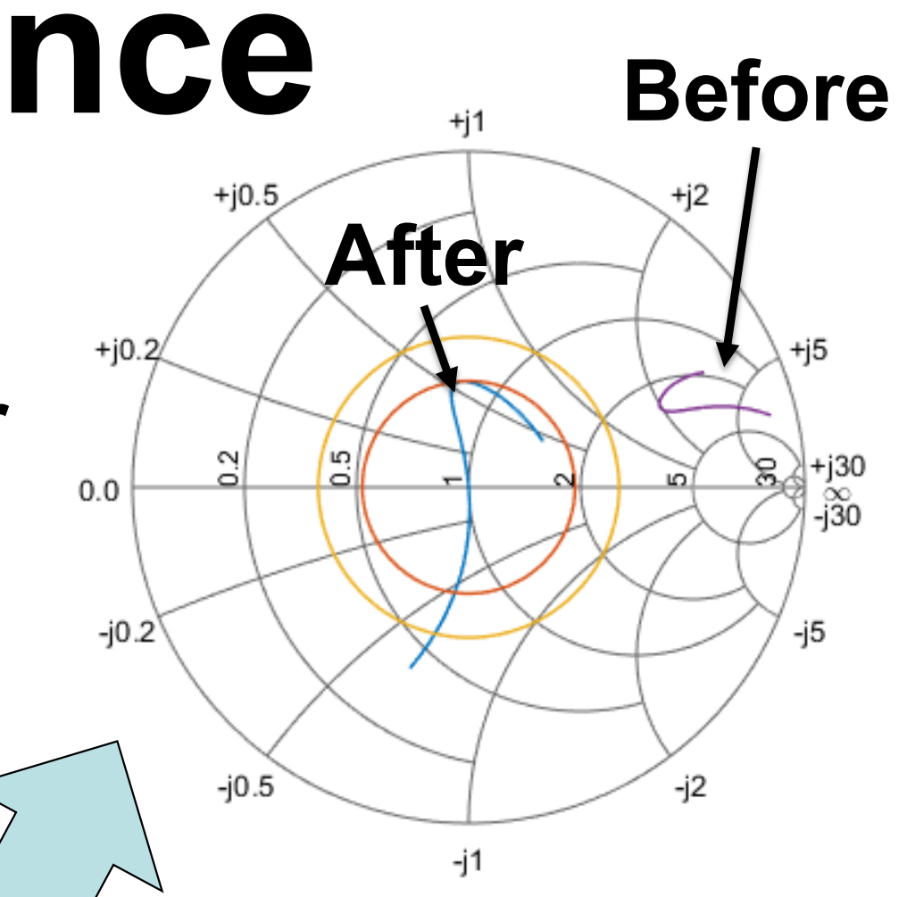
Board construction and photo by Tanuj Sen

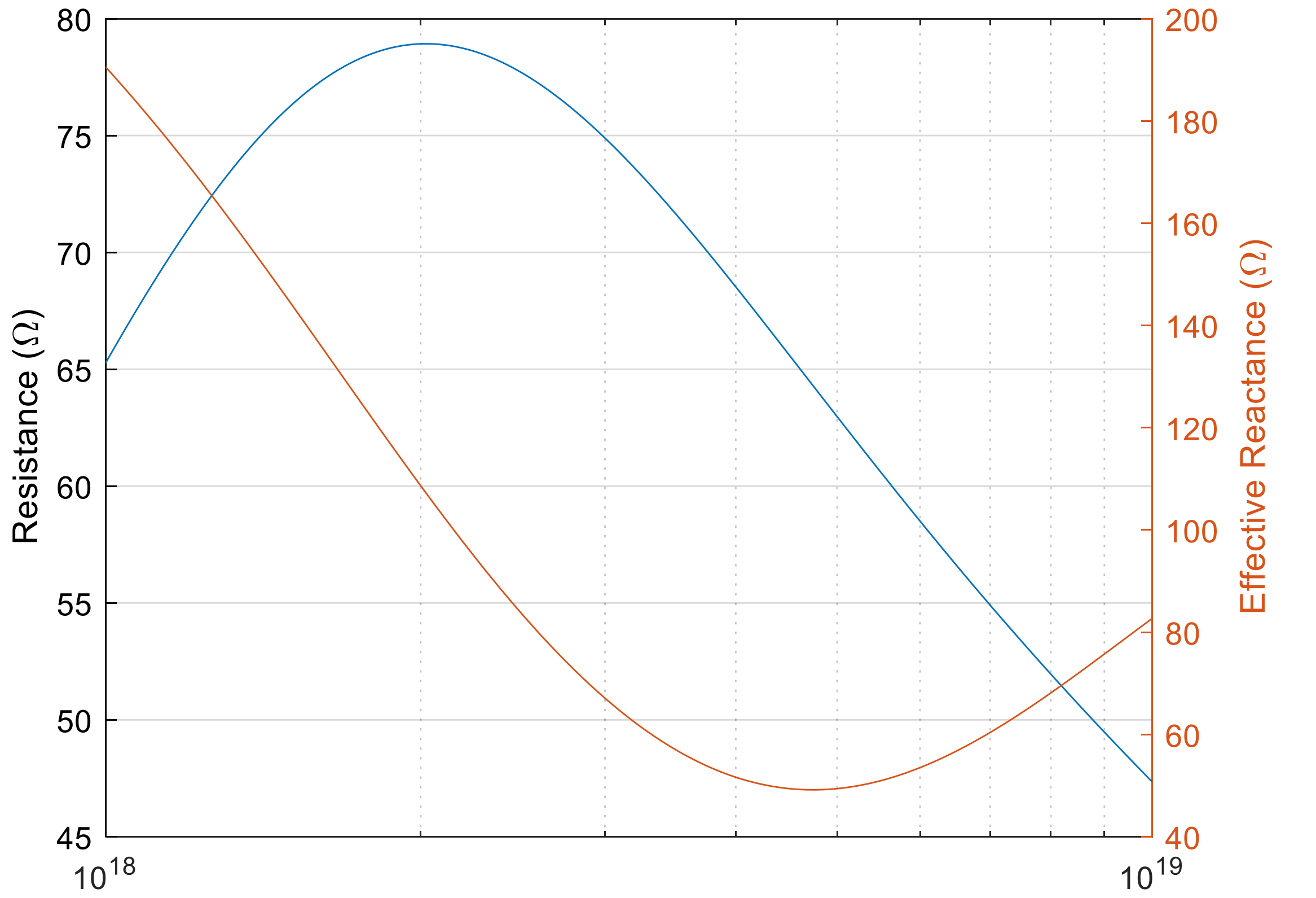
ZVS: Zero Voltage Switching

Modeling the Plasma Impedance

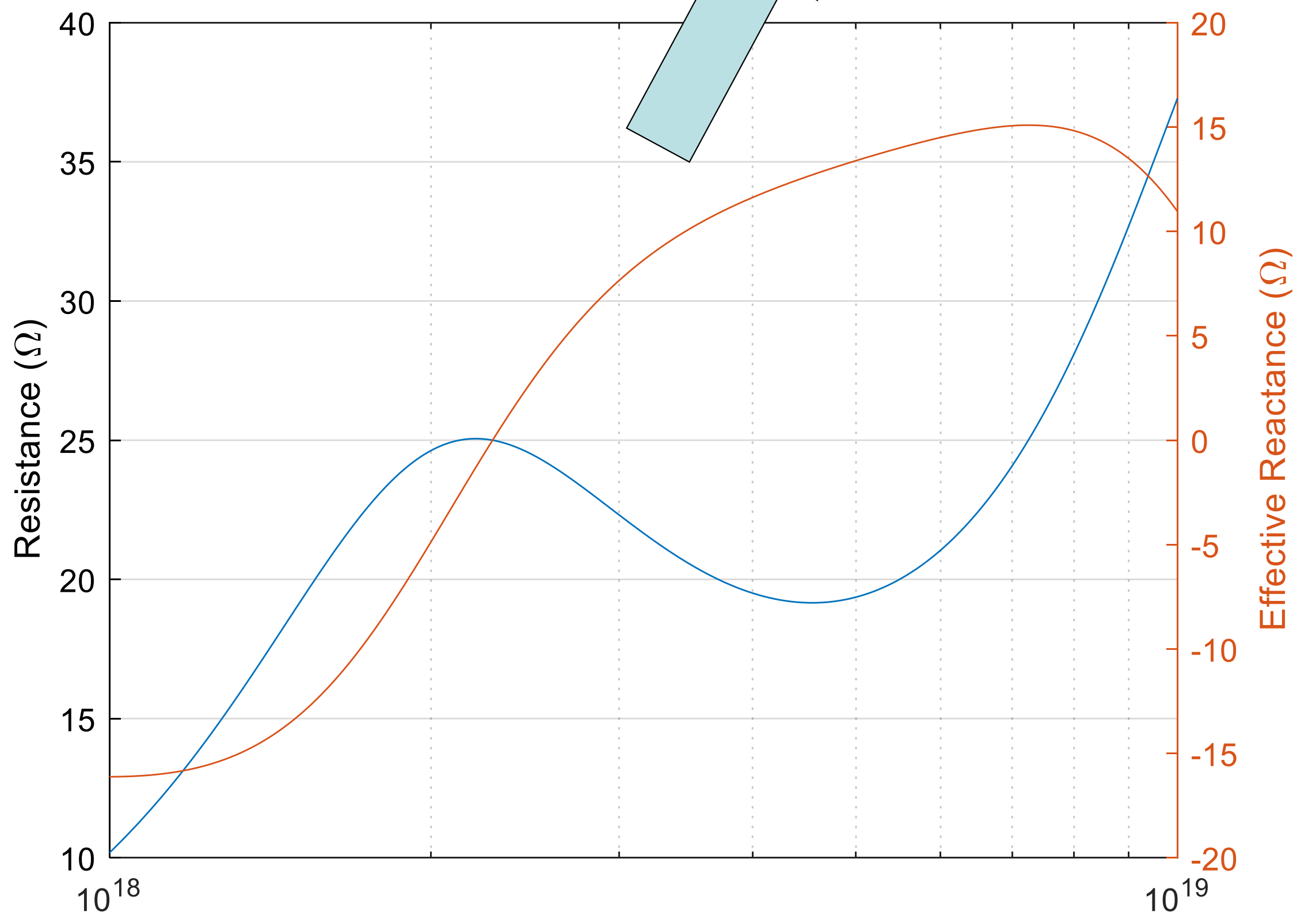
- Inductively Coupled Plasma (ICP) coil used for heating plasma
- ICP impedance is dynamically variable depending on the electron density, pressure, temperature etc.

After matching network, power reflection is drastically reduced





The total resistance and reactance of the plasma chamber varies considerably with varying electron density (pressure and temperature constant)



Adding a matching network reduces the variation of the plasma impedance and reduces the power reflection due to mismatched source and load impedances

ARPA-E Innovation Summit, March 22-24, 2022 National Harbor, MD USA

Work funded by ARPA-E GAMOW Under Grant DE-AR0001372

Princeton FUSION SYSTEMS

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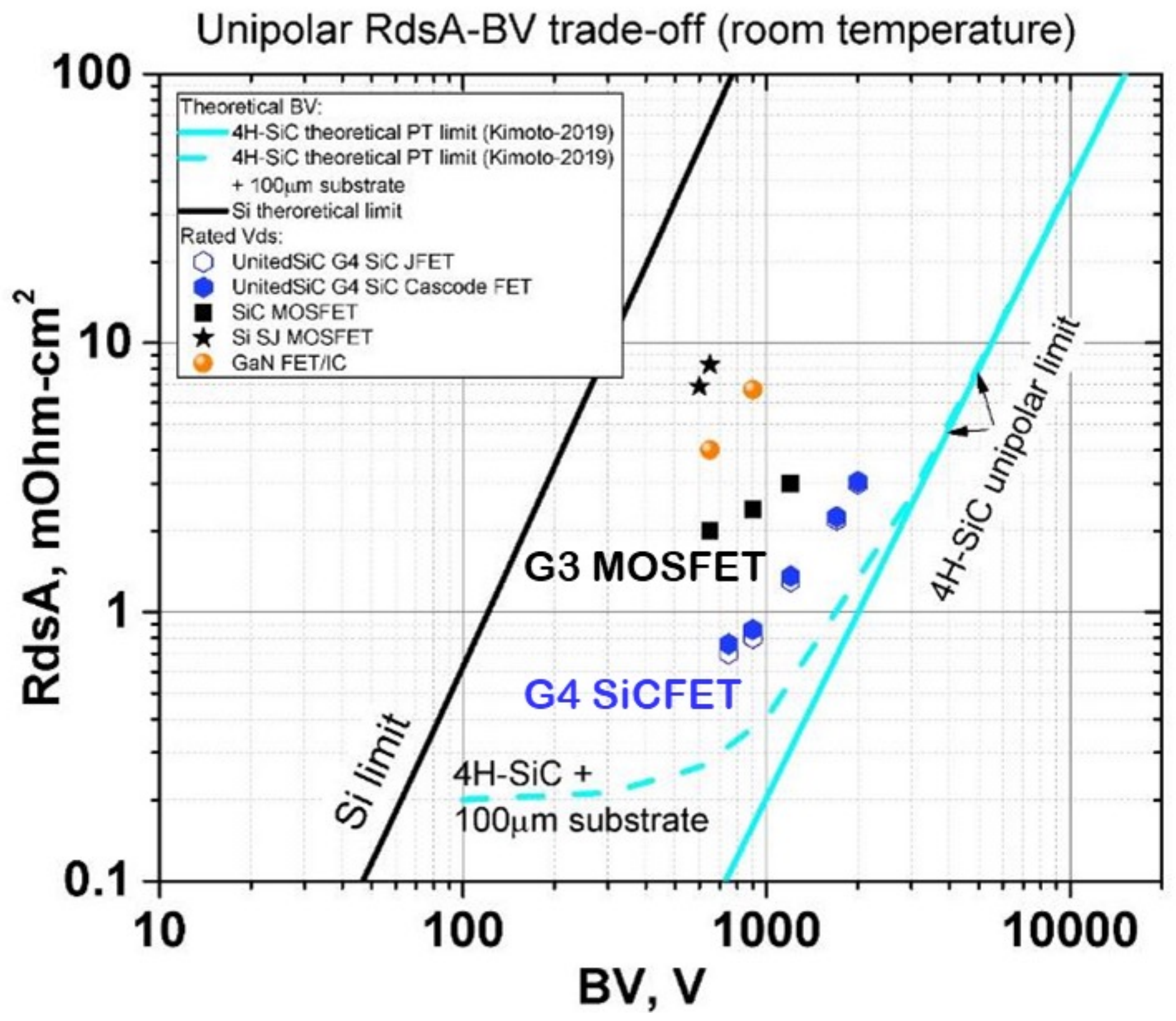
2 kV SiC Cascode FETs



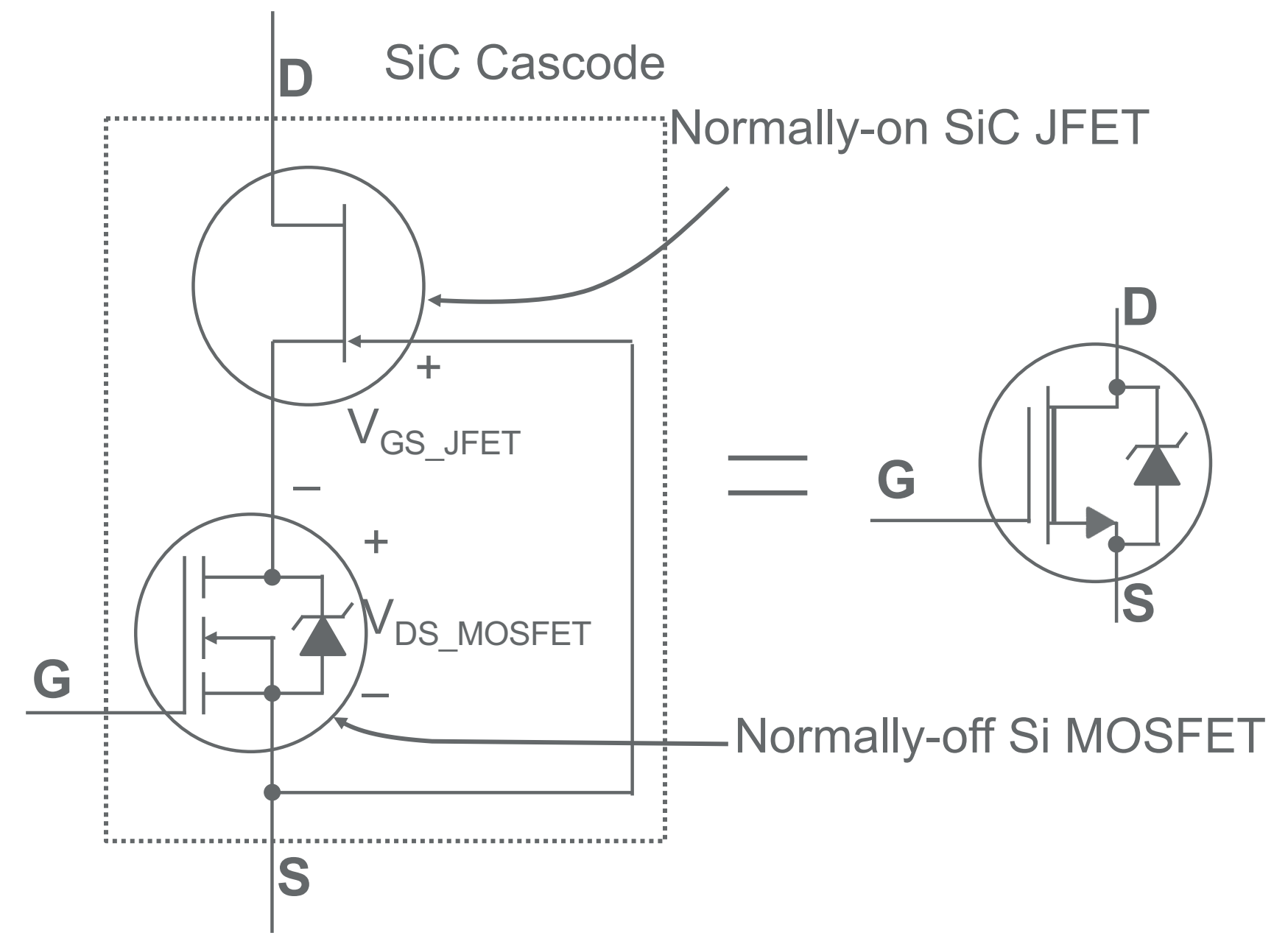
WBG Devices offer unprecedented performance for high-voltage, high-frequency power electronics

SiC's benefits include:

- 10x higher critical electric field than Si
- 3x better thermal conductivity
- Higher temperature operation due to wide bandgap
- 10-100x Lower on-resistance, single carrier (faster) devices up to 10kV range

Qorvo offers lowest R_{On} x Area switch using cascode technology of:

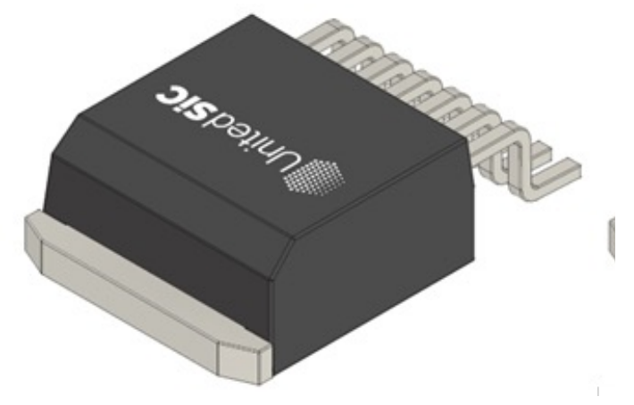
Low Voltage Si MOSFET + High Voltage SiC JFET



SiC Cascode Benefits include:

- Excellent voltage scaling (2kV developed in this program)
- Smaller die size compared to conventional SiC options
- 0-10V, 0-12V gate drive voltage for ZVS applications
- Lower gate charge Qg x $R_{DS,On}$ than conventional SiC options, reduced driver losses
- Lower output capacitance for reduced switching losses and high-frequency switching

This Work:

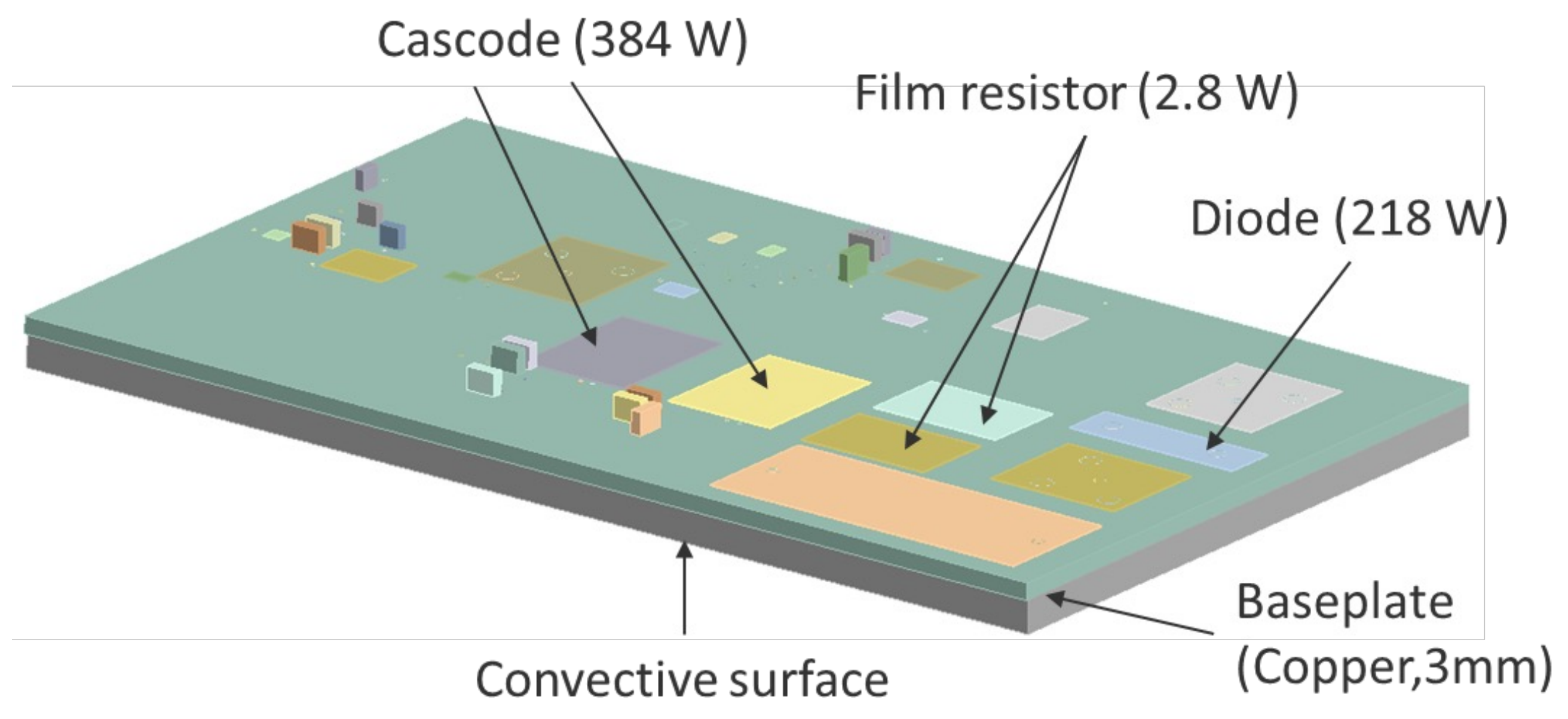


- Developed new 2kV (BV=2.4kV) SiC VJFET with *record low* specific on-resistance of 2.95mOh-cm^2, allowing reliable operation with V_{DC}=1.5kV
- Developed a normally-Off 2kV/60mOhm Stacked-Cascode SiC FET in low inductance Surface Mount discrete package (D^{2}Pak7L) with:
  >50% lower R_{On}·Qg, 50% Lower R_{On} · Eoss, 18% Lower R_{On} · Coss(tr) than latest 2kV commercial SiC MOSFETs

Load switch board thermal analysis

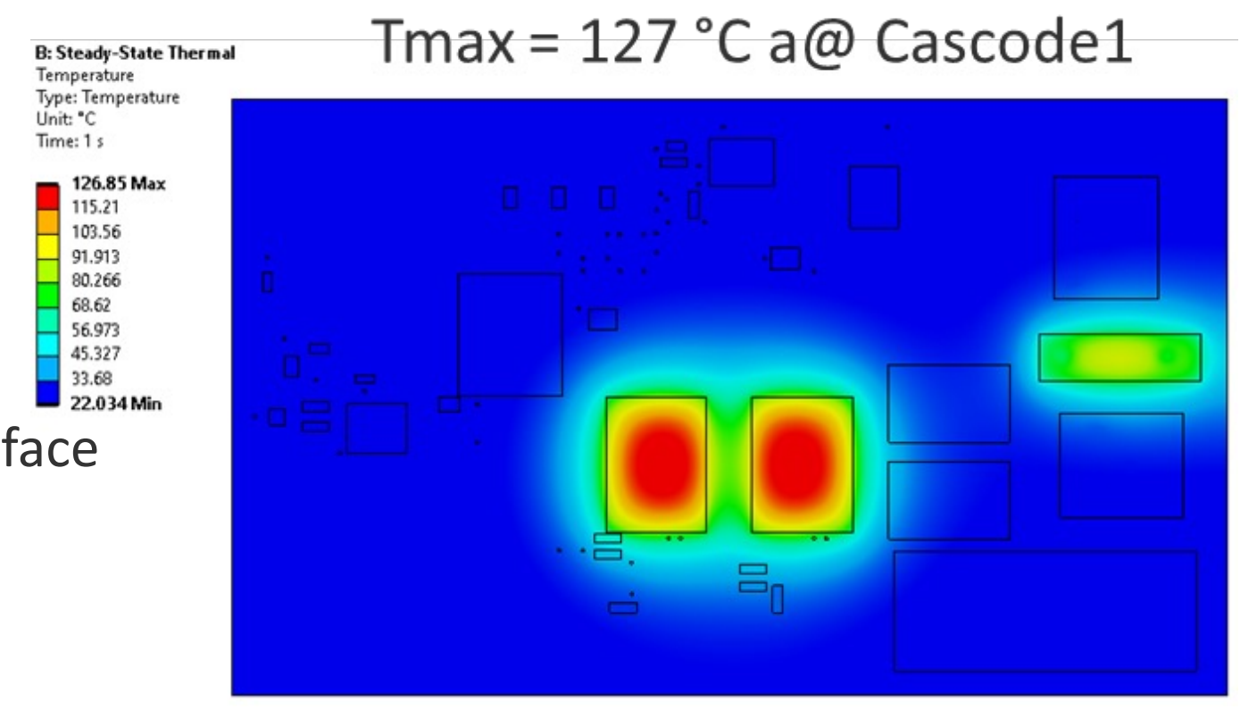
Load switch board design

- Two cascode devices with 384 W heat
- One diode with 218 W heat
- Heat losses from other components are negligible
- A 3-mm-thickness copper base plate is added as heat spreader
- Bottom side is used for cooling

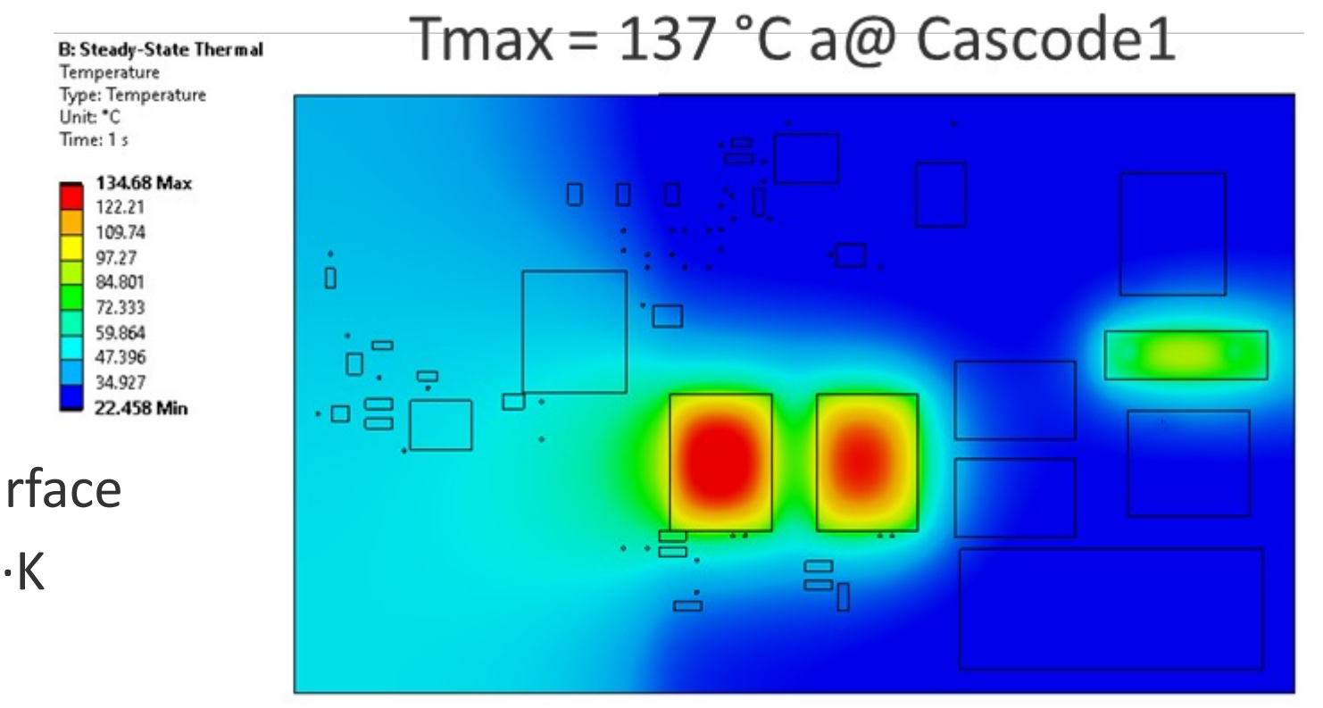


Parametric study

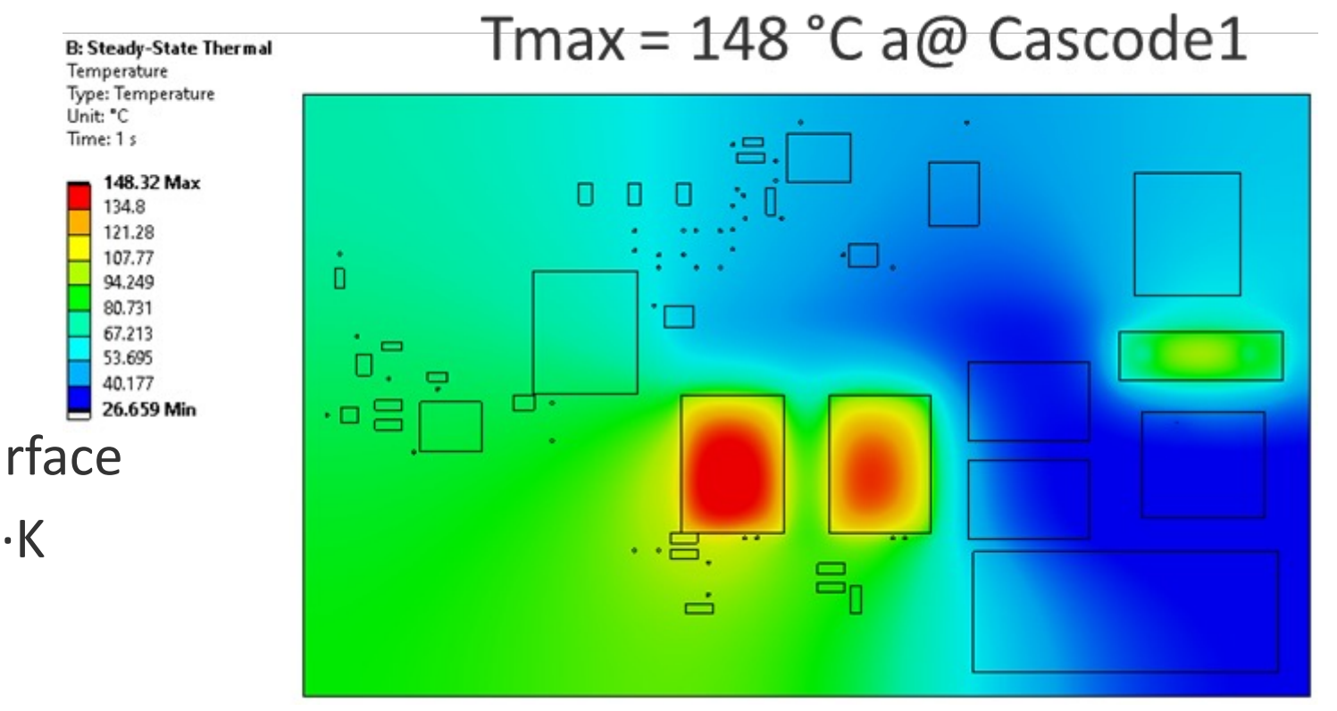
- Heat transfer coefficient (HTC)
- PCB effective thermal conductivity k_{eff}
- Convective surface area
- Thermal interface materials (TIM)


Tmax = 127 °C a@ Cascode1

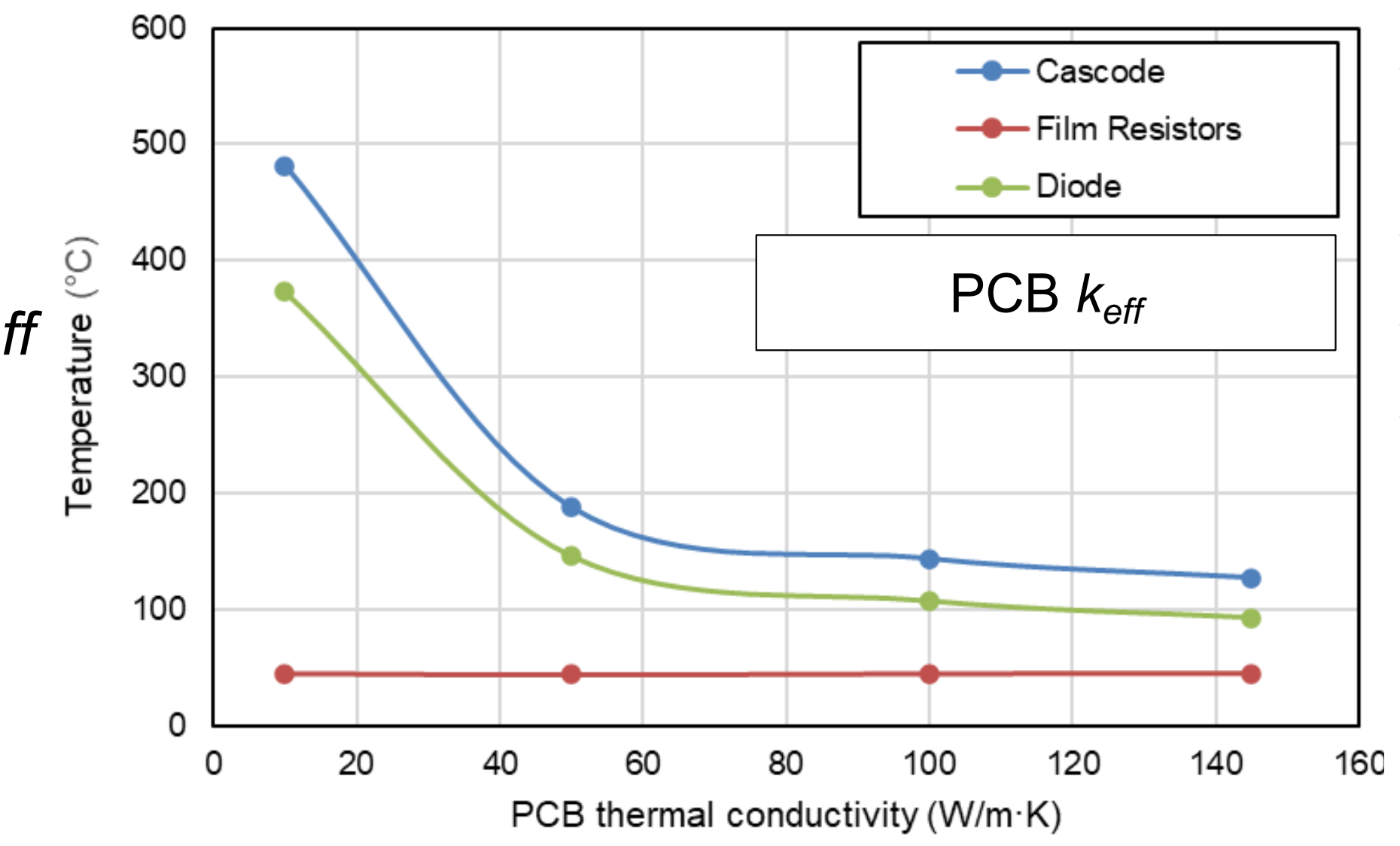
- 104 x 62 mm^2 baseplate surface
- PCB effective k: 150 W/m·K
- HTC: 30,000 W/m^2·K
- T: 22°C


Tmax = 137 °C a@ Cascode1

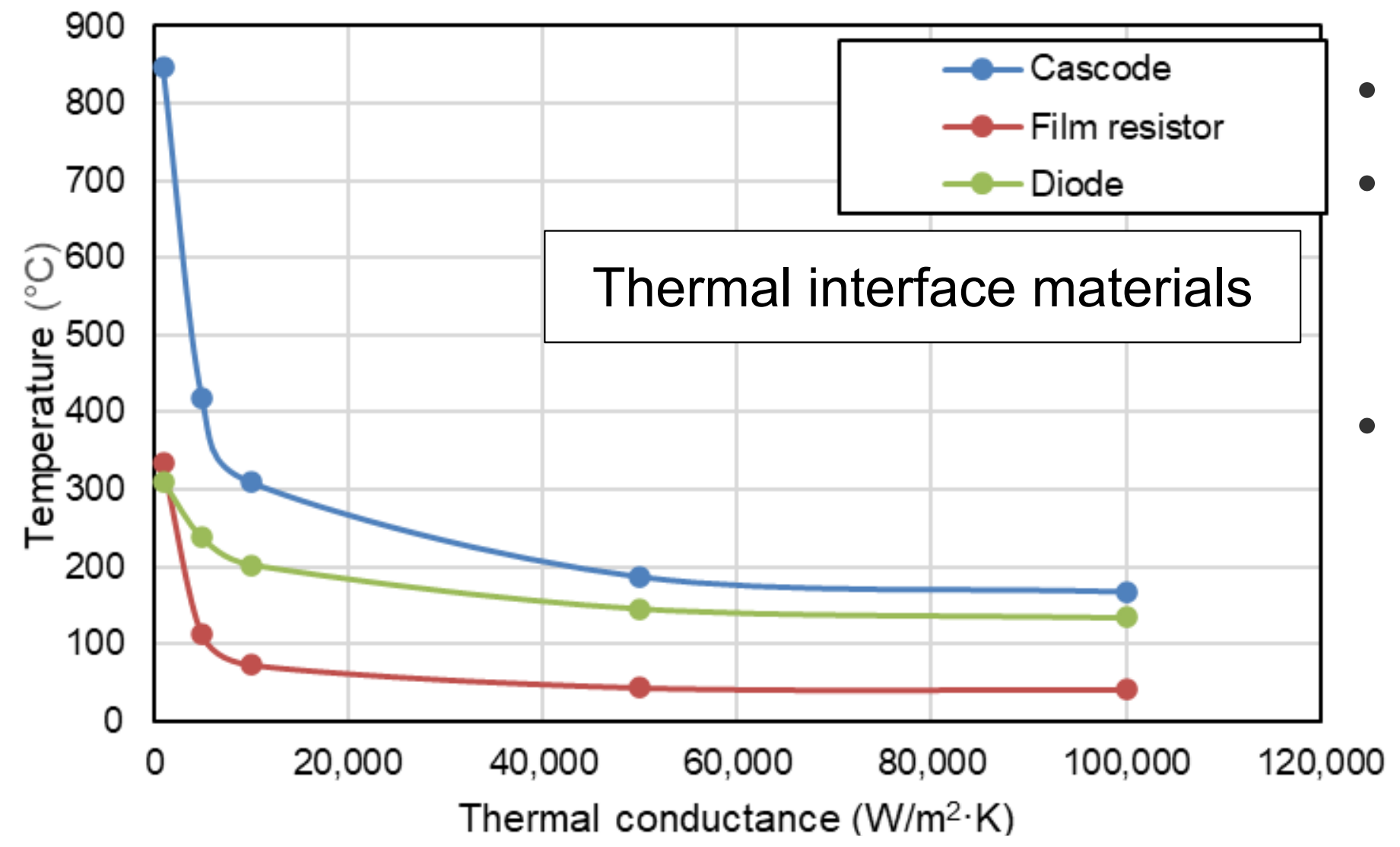
- 66 x 62 mm^2 baseplate surface
- PCB effective k: 150 W/m·K
- HTC: 30,000 W/m^2·K
- T: 22°C


Tmax = 148 °C a@ Cascode1

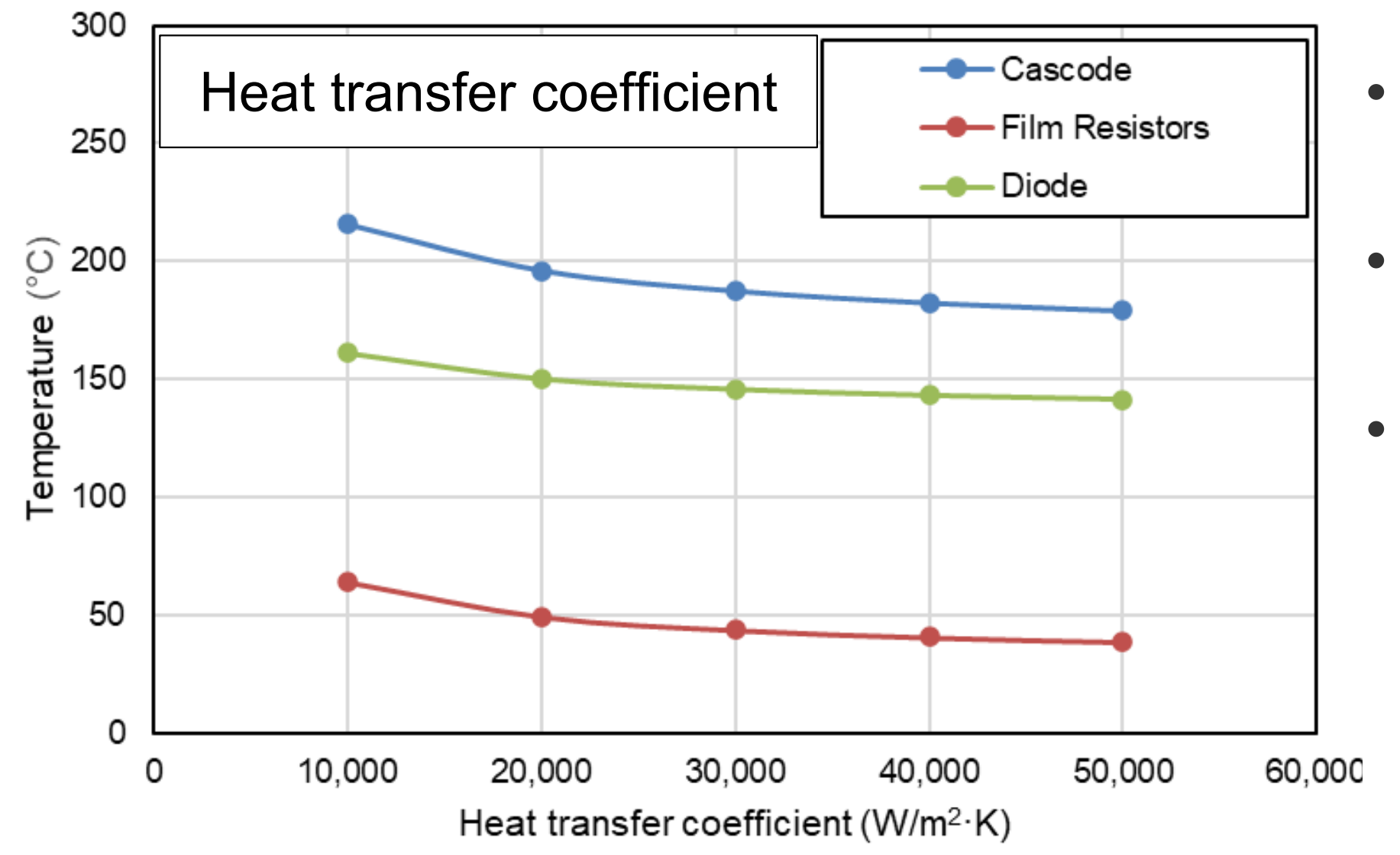
- 66 x 24 mm^2 baseplate surface
- PCB effective k: 150 W/m·K
- HTC: 30,000 W/m^2·K
- T: 22°C



- 104 x 62 mm^2 baseplate surface
- HTC: 30,000 W/m^2·K
- T: 22°C
- PCB k needs to be higher than 50 W/m^2·K to provide device temperature lower than 200°C.



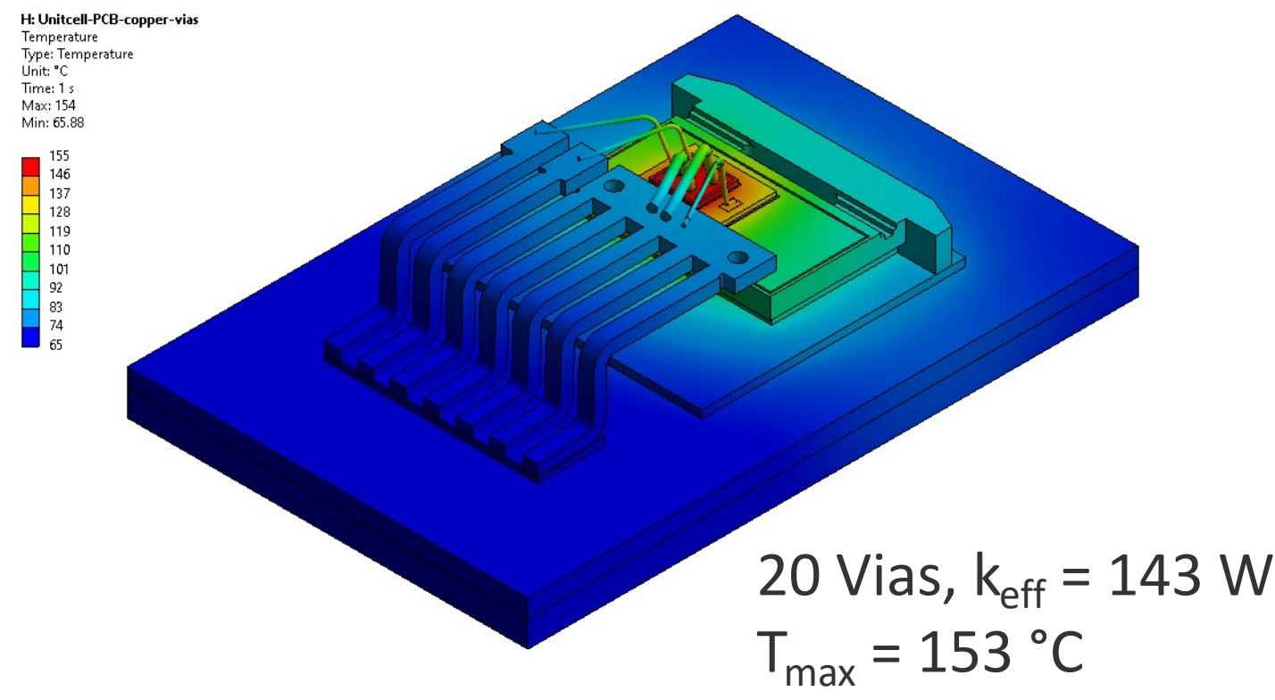
- PCB k = 50 W/m·K
- TIM has significant impact on device temperature.
- Thermal conductance must be higher than 50,000 W/ m^2·K



- 104 x 62 mm^2 baseplate surface
- Effective PCB k: 50 W/m·K.
- HTC must be higher than 30,000 W/ m^2·K to provide device temperature lower than 200°C.

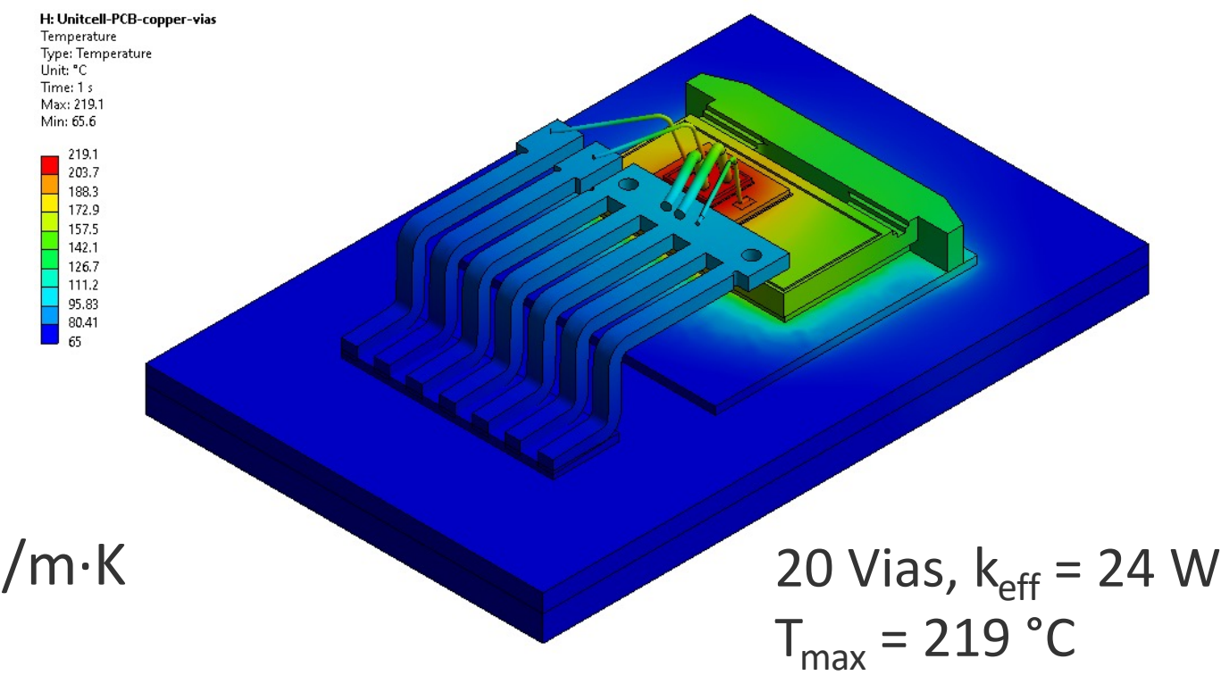
High performance PCB board

- Use AlN as core material
- Deploy abundant number of vias



20 Vias, k_{eff} = 143 W/m·K
T_{max} = 153 °C

- AlN core materials
- HTC: 30,000 W/m^2·K
- T: 65°C



20 Vias, k_{eff} = 24 W/m·K
T_{max} = 219 °C

- Conventional core materials, e.g., FR4
- HTC: 30,000 W/m^2·K
- T: 65°C

Simulations performed by Dr. Xuhui Feng

ARPA-E Innovation Summit, March 22-24, 2022 National Harbor, MD USA

Work funded by ARPA-E GAMOW Under Grant DE-AR0001372